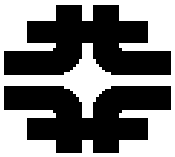
ADMEM Checkout
Phase 2
Technician Name _____
ADMEM Serial Number _____



Fermilab

Particle Physics Division/CDF Upgrade Project

ADMEM
ADC/Memory Module

CHECKOUT DOCUMENT

Revised
5/26/99
Theresa M. Shaw
Rodney Klein

Checkout Sheet
Technician Name: _____
ADMEM #: _____

Note any test which initially fails and the action taken to repair it:

Name of Failing Test: _____
Repair Steps: _____
_____
_____
_____
_____
_____
_____

Name of Failing Test: _____
Repair Steps: _____
_____
_____
_____
_____
_____
_____

Name of Failing Test: _____
Repair Steps: _____
_____
_____
_____
_____
_____
_____

Name of Failing Test: _____
Repair Steps: _____
_____
_____
_____
_____
_____
_____

Name of Failing Test: _____
Repair Steps: _____
_____
_____
_____
_____
_____
_____

Name of Failing Test: _____
Repair Steps: _____
_____
_____
_____
_____
_____
_____

Name of Failing Test: _____
Repair Steps: _____
_____
_____
_____
_____
_____
_____

Name of Failing Test: _____
Repair Steps: _____
_____
_____
_____
_____
_____
_____

Name of Failing Test: _____
Repair Steps: _____
_____
_____
_____
_____
_____
_____

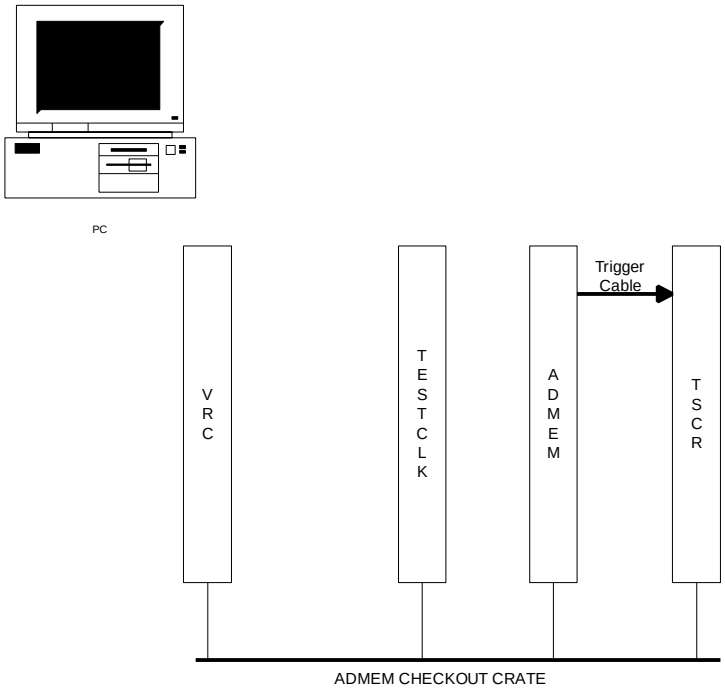
Name of Failing Test: _____
Repair Steps: _____
_____
_____
_____
_____
_____
_____

Name of Failing Test: _____
Repair Steps: _____
_____
_____
_____
_____
_____
_____

TESTSTAND EQUIPTMENT

Each Teststand should be equipped with the following Equipment:

- VIPA CDF Crate
- VME CPU on 9U adapter
- TSCR
- TESTCLK_V7
- Short Trigger Cable
- Special Digital Paddle Card with Testpoints
- 20 Digital Paddle Cards
- Digital Multimeter
- Oscilloscope
- HP Logic Analyzer



02/02/99 14:12:05 Electronics Design System
Bill of Materials
<<<From Job: D:\PPD_Jobs\ADMEM_P_V3\vbdc\ADMEM_P_V3.prj>>>

Fermi National Accelerator
PPD/ET&T/CDF Upgrade Project

Item	QTY	vendor part number	Description	Cost	REF D
1	1	AD760AQ	Analog Devices 16/18 bit Self-Calibratin		U114
2	1	AD826AR	Analog Devices High Speed Low Pwr Dual O		U117
3	1	AMP 352009-1 PLUS SHIELDS .	AMP 5x19 Z-PACK 2mm Female Conn w/gnd sh	18.75	P0
4	8	AMP 536272_1.	AMP 536272_1 40 pin micro_strip male 536	16.00	J3-J16
5	1	AM27S19SAPC	32x8 PROM	1.25	U5
6	1	AM29F200B-75EC	2Mb 5.0V Flash	10.00	U23
7	7	Am29F100B-75EC	1 Mb CMOS Flash Memory	15.00	U50,U
*					U58-U6
8	1	BOT d_strip	Bottom Discharge strip	.01	X8
9	1	C&K P8121 1160-1890	Mom. Push button Panel mnt	2.48	S1
10	20	CAFE_MODULE	Analog Cafe Module		PB1-P
11	28	COTTER PIN	test point	0.01	TP28,
*					TP73-
*					TP134
*					TP144
*					TP153
12	2	CY7B991-7JC	ROBOCLOCK	21.85	U65,U
13	2	CY7C470-15JC	Cypress 8K x 9 FIFO	22.00	U3,U1
14	10	CY74FCT16374CTPAC	16-bit register	3.45	U20,U
*					U41-U4
*					U98-U9
15	1	CY74FCT16500TTSSOP	18-bit Registered Transceivers	5.78	U28
16	28	CY74FCT16543CTPAC	16-bit latched tranceiver	5.25	U36,U3
*					U44-U4
*					U78-U
17	9	CY74FCT162244TTSSOP	16-Bit Buffers/Line Drivers	3.95	U4,U4
*					U55-U5
*					U104
18	18	DS90C031T	LVDS Driver	2.23	U14,U
*					U34-U6
*					U73-U7
*					U102-U
*					U112-U
19	4	DS90C031TM	LVDS QUAD CMOS DIFF LINE DRVR		U106,
*					U113
20	6	ERIE 8121-050-651-103M 1415-3000	Bypass Cap .01UF	0.07	C26,C
*					C45-C4
21	1	ERIE 8131-100-651-153M 1415-3090	Bypass Cap .015UF	0.07	C16
22	3	ERJ-8ENF1.00K Digi P1.00KFBK-ND	1/8W 1% 1.0K ohm	0.0542	R4,R1
23	17	ERJ-8ENF82.5 Digi P82.5FBK-ND	1/8W 1% 82.5 ohm	0.0542	R13,R
*					R25-R2
*					R32-R3

02/02/99 14:12:05 Electronics Design System
Bill of Materials
<<<From Job: D:\PPD_Jobs\ADMEM_P_V3\vbdc\ADMEM_P_V3.prj>>>

Fermi National Accelerator
PPD/ET&T/CDF Upgrade Project

Item	QTY	vendor part number	Description	Cost	REF D
*					R44,R4
*					R52
24	17	ERJ-8ENF100 Digi P100FBK-ND	1/8W 1% 100 ohm	0.0542	R54,R
25	17	ERJ-8ENF124 Digi P124FBK-ND	1/8W 1% 124 ohm	0.0542	R9,R1
*					R24,R2
*					R33,R3
*					R45,R4
26	1	ERJ-8ENF267 Digi P267FBK-ND	1/8W 1% 267 ohm	0.0542	R5
27	4	ERJ-8ENF909 Digi P909FBK-ND	1/8W 1% 90.9 ohm	0.0542	R34,R
28	7	FCN-235D020-G/E(MH)	Fujitsu 20 Pin SCSI II	2.20	P4-P1
29	120	Ferronics FMB12061201	Ferrite Bead		FE1-F
30	3	HARTING-0201-160-2101	VME64 Card Connector	25.29	P1-P3
31	6	HP HLMP-1301 1445-0475	Red LED	0.24	D1,D3
32	2	HP HLMP-1401 1445-0495	Yellow LED	0.24	D2,D5
33	2	JUMP3	Three Pin Jumper	0.10	J1,J2
34	7	KEMET T354H336K016AS	33UF 16V RADIAL Dip	0.68	C17,C
*					C37,C4
35	4	LITTLEFUSE 251002 1120-0235	2 AMP PCB Fuse	0.74	F3-F6
36	2	LITTLEFUSE 251010 Newark 20F604	10 AMP PCB Fuse	0.74	F1,F2
37	2	MACH 110-12JC	AMD PLD 44 Pin PLCC	7.00	U12,U
38	1	MC10H350P	PECL to TTL Translator	7.98	U72
39	4	MOTOROLA 1N5908	Transient Suppressor 6.0V	1.24	D6-D9
40	2	Motorola 1N6277A	Transient Suppressor 18V	0.70	D10,D
41	5	Murata BNX002-01	EMI Supression Filters	5.00	BF1-BI
42	4	M833 Custom	No PDB description available		X2,X4
43	1	PAN ECS-H1CY105R DIG PCT3105	SMT CAP 1.0UF	0.3955	C53
44	143	PAN ECSH1DC106R	SMT CAP 10.0UF	0.9765	C1-C1
*					C20-C
*					C32,C3
*					C40-C
*					C52,C5
*					C62-C
*					C91-C
*					C115-
45	1	PAN ECU-V1H103KBG DIG PCC103BN	SMT CAP 0.01UF	0.168	C50
46	315	PAN ECU-V1H104KBW DIG PCC104B	SMT CAP 0.1UF	0.5914	C60,C
*					C84-C
*					C112,C
*					C175-
47	1	PAN ECU-V1H560JCG DIG PCC560CG	SMT CAP 56pF	0.133	C89
48	5	RC05-270 1487-0290	270 ohm 1/8W 5%	0.19	R1,R6
49	1	RC05-820K 1487-0497	1/8W 820Kohm 5%	0.18	R8

02/02/99 14:12:05 Electronics Design System
Bill of Materials
<<<From Job: D:\PPD_Jobs\ADMEM_P_V3\vbdc\ADMEM_P_V3.prj>>>

Fermi National Accelerator
PPD/ET&T/CDF Upgrade Project

Item	QTY	vendor part number	Description	Cost	REF D
50	3	RC07-1.5M 1487-1125	1/4W, 5PCT, THRU	0.14	R3,R1
51	1	RC07-5.6 Digi 5.6QBK-ND	1/4W, 5PCT, THRU	0.06	R11
52	4	RC07-1000	1/4W, 5PCT, THRU	0.08	R58-R
53	4	RC07-4700 1487-0825	1/4W, 5PCT, THRU	0.08	R2,R1
54	2	RN55C-820	1/8W 1PCT Thru	.04	R62,R6
55	6	SN74ABTE16245SSOP	16 Bit Incident Transceiver	5.60	U7,U1
*					U75U1
56	1	SPARE_RES_SMT_0805	Spare	0.00	R64
57	5	Samtec TSW-12-07-L-D 2pin sip	2 pin jumper - mates with SNT-100-BK-G $	0.16	S2-S6
58	4	Spare-IC 24DIP3	Spare Part	0.00	U8-U1
59	116	TEST_PIN	.025 x .025 square post.	.01	TP1-T
*					TP15-
*					TP26T
*					TP31-
*					TP43-
*					TP56-
*					TP84-
*					TP120
*					TP137
*					TP141
60	1	TOP d_strip	Top Discharge strip	.01	X1
61	4	XC4003EPQ100-3	Xilinx FPGA XC4003E	45.75	U24,U2
62	6	XC4013EPQ240-3	Xilinx FPGA XC4013EPQ240	293.60	U18,U6
63	2	XC17128-PD8C	Xilinx Serial PROM	9.70	U25,U3
64	1	XC17256-PD8C	Xilinx Serial PROM	15.10	U6
65	2	shunt10 AMP 1-435704-0	10 position shunt	0.62	U17,U
66	2	slpbar	No PDB description available		X3,X7
67	1	1N5817	Shotky diode 1Amp 20V	.80	D4
68	1	3D7408-1	Data Delay Devices 267ns delay, 1ns step	35.00	U105
69	3	10x-2-102	Bourns 10 pin 1K SIP pin 1 common	0.34	RP1-RI
70	1	74F38N	Nand gate, OC output	0.53	U33
71	1	74LS14N 1455-8014	Hex Scmitt-trigger Inverters	0.31	U2
72	1	74LS123N 1455-8123	Multivibrator	0.35	U1
73	1	016-2008-00-0-200 1460-1600	Test point, BLACK	0.85	TP152
74	1	016-2008-00-0-203 1460-1700	Test point, ORANGE	0.58	TP151
75	1	016-2008-00-0-205 1460-1680	Test point, GREEN	0.98	TP149
76	1	016-2008-00-0-206 1460-1620	Test point, BLUE	0.85	TP150
77	1	016-2008-00-0-208 1460-1660	Test point, GRAY	0.89	TP147
78	1	2743021446 PSC ELECTRONICS	SMT FERRITE BEAD 10UH	1.30	L1

Total Parts Used: 1026
Total Parts Cost: 3164.38

Initial Checkout

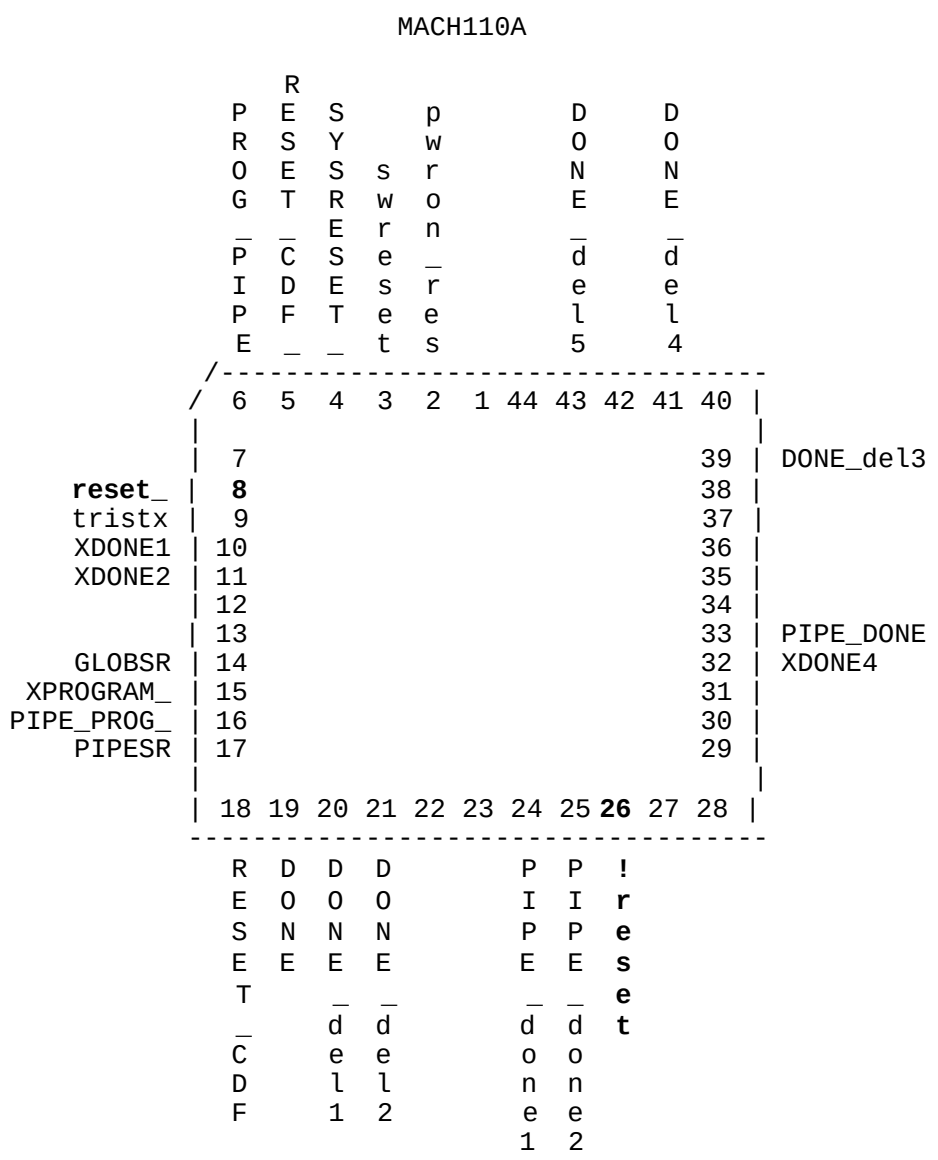
_____ Verify that the module has been through initial checkout.

For Reference, the Bill of Materials (BOM) is included in previous pages.

Check functioning of RESET Switch

_____ Check the RESET PLD. **U15-8** (page 4A) should be high and go low when the front panel reset switch is depressed. **U15-26** should be low and go high when the reset switch is depressed.

NOTE: U15 is rotated 180 degrees on the board



Check for Xilinx Download

If the Xilinx download is successful, the following pins should be high.

_____ VME Slave **U6-4** (page 3A)

_____ FLASH Control **U30-4** (page 3B)

_____ Download **U25-4** (page 16D)

Check Ready and Plug LEDs

_____ At this point, the Pipeline FPGAs have not been downloaded. Make sure the READY LED **D3** (green, page 16) and the PLUG LED **D5** (green, page 20A) are off.

Check of ADMEM Registers

Please Note that many ADMEM registers will not testable until the Pipeline FPGA chain has been successfully downloaded.

Go into VASE, and

_____ Map the crate and verify that the ID PROM **U5** (page5) of the ADMEM reads out in the correct slot and of a form similar to that below.

0001 003 ADMEM_V4.0

The first number (0001) in the example should match the engraved board number, the rest of the field should read as the example does.

_____ Verify that the Select (yellow) indicator, **D2** (page3) comes on when the board is addressed and turns off when it is not.

Go to the ADMEM Checkout Menu and

_____ **Option 1** - Test the Diagnostic Register. Located in the VME Slave FPGA **U18** (page 3A).

_____ **Option 2** - Test the Control Register. Located in the VME Slave FPGA **U18** (page 3A).

_____ **Option 3** - Test the Access Register for FLASH RAM. Located in the VME Slave FPGA **U18** (page 3A).

_____ **Option 4** - Test the Flash RAM Select Register. Located in the VME Slave FPGA **U18** (page 3A).

_____ **Option 5** - Test the Pipeline Diagnostic Channels Enable Register. Located in the VME Slave FPGA **U18** (page 3A).

_____ **Option 6** - Test the Diagnostic Pipeline Data FIFO - **U3** and **U16** (page 5).

_____ **Option 7** - Test the Transition Port Register - **U28** (page 24).

Checkout of Flash RAM spaces

There are 28 Flash RAM spaces on the ADMEM module. The first twenty spaces are allocated to the CAFE modules, the next 7 to the trigger sum lookup tables, and the final space is for downloading the pipeline FPGAs.

Channel 0-19 (0x0 – 0x13) map to Café Modules 0-19
Channel 20-26 (0x14 – 0x1A) map to trigger sum lookup table (0-6)
Channel 27 (0x1B) maps to Pipeline FPGA Download

To Check the CAFE Module Address Space, rlogin to crate controller. At the prompt, type
ld <anadmem.o,
this loads the crate controller with the anadmem object code. Then type
cd "pathname to your test directory",
make sure the quotes are around the directory pathname. Then type
anadmem_menu
to start the program.

Make sure test directory is read/writeable to the world. To do this, go back one directory and type **chmod 777 "directory name"**

_____ Load the ADMEM with Digital Paddle Cards.

_____ Make sure TESTCLK backplane jumpers are set.

Trigger Sum Flash RAMs

_____ Select **Option 8 - Trigger Sum Flash Ram Test** from the **Checkout Menu**
This test is done automatically, user needs to check screen for errors and verification of the below steps:

- "Enable VMEbus access to Flash RAM data lookup tables" in the Control Register is set.
- Write BEAD (hex) to the Access Register for Flash RAM.
- Write a 14 (hex) to the Flash RAM select register to test Flash RAM **U62** (page 16C).
- step A. Erase the Flash RAM
- step B. now download sequential data to the FLASH RAM
- step C. verify the sequential download.
- Step D. download pattern data to the FLASH RAM
- Step E. Verify the pattern download.
- Write a 15 (hex) to the Flash RAM Select register. Test Flash RAM **U60** (page 17B) by repeating steps A thru E.
- Write a 16 (hex) to the Flash RAM Select register. Test Flash RAM **U58** (page 18B) by repeating steps A thru E.

- Write a 17 (hex) to the Flash RAM Select register. Test Flash RAM **U56** (page 19B) by repeating steps A thru E.

- Write a 18 (hex) to the Flash RAM Select register. Test Flash RAM **U54** (page 20B) by repeating steps A thru E.

- Write a 19 (hex) to the Flash RAM Select register. Test Flash RAM **U52** (page 20C) by repeating steps A thru E.

- Write a 1A (hex) to the Flash RAM Select register. Test Flash RAM **U50** (page 20D) by repeating steps A thru E.

Program Download Flash RAM will be tested.

_____ Select **Option 9** - **Program Download Flash Ram Test** from the **Checkout Menu**
This test is done automatically, user needs to check screen for errors and verification of the below steps:

- “Enable VMEbus access to Flash RAM data lookup tables” in the Control Register is set.
- Write BEAD (hex) to the Access Register for Flash RAM.
- Write a 1B (hex) to the Flash RAM Select register. This tests **U23** (page 16).
- step A. Erase the Flash RAM
- step B. now download sequential data to the FLASH RAM
- step C. verify the sequential download.
- Step D. download pattern data to the FLASH RAM
- Step E. Verify the pattern download.

Test of downloading Pipeline FPGA from Flash RAM

_____ Select **Option 10 - Pipeline Download S-Record Test** from the **Checkout Menu**
The program will do the first part automatically except for the file name which is done interactively.

- Now, we will download the Flash RAM which will be used to program the Pipeline FPGA.
- Set the "Enable VMEbus access to Flash RAM data lookup tables" in the Control Register.
- Write BEAD (hex) to the Access Register for Flash RAM.
- Write a 1B (hex) to the Flash RAM Select register.
- Erase, Download and Verify Motorola S-records, download the file /home/usr1/tshaw/plug_v3.exo
- When download is complete, the program will turn off the "Enable VMEbus access to Flash RAM data lookup tables" in the Control Register.
- Toggle the "Program Pipeline" bit high then low in the Control register.
- If the download was a success, the front panel READY (green) indicator, **D3** (page16) should be on.

_____ Verify that the PLUG (green) indicator, **D5** (page 20A) is on.

_____ Now verify Front Panel Reset switch will download the Pipeline FPGA - Push the RESET button. The READY and PLUG LEDS should turn off briefly.

_____ The front panel READY (green) indicator, **D3** (page16) should be on.

_____ Verify that the PLUG (green) indicator, **D5** (page 20A) is on.

_____ Finally, verify that a power-up reset will produce a proper download. Pull the board out of the crate and re-insert it.

_____ The front panel READY (green) indicator, **D3** (page16) should be on.

_____ Verify that the PLUG (green) indicator, **D5** (page 20A) is on.

TESTING CAFÉ Flash RAM Paths – Using Digital Paddle Cards

_____ Select **Option 11 – Digital Paddle Card Flash Ram Test** from the **Checkout Menu.**
This test is done automatically, user needs to check screen for errors and verification of the below steps:

- Enable the TESTCLK backplane clock.
- "Enable VMEbus access to Flash RAM data lookup tables" in the Control Register is set.
- Write BEAD (hex) to the Access Register for Flash RAM.
- Write a 00 (hex) to the Flash RAM select register and insert a Digital Paddle board in module slot PB20.
- step A. Erase the Flash RAM
- step B. now download sequential data to the FLASH RAM
- step C. verify the sequential download.
- Step D. download pattern data to the FLASH RAM
- Step E. Verify the pattern download.
- Next write 01 (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB19 and repeat steps A thru E above.
- Next write 02 (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB18 and repeat steps A thru E above.
- Next write 03 (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB17 and repeat steps A thru E above.
- Next write 04 (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB16 and repeat steps A thru E above.
- Next write 05 (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB15 and repeat steps A thru E above.
- Next write 06 (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB14 and repeat steps A thru E above.
- Next write 07 (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB13 and repeat steps A thru E above.
- Next write 08 (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB12 and repeat steps A thru E above.
- Next write 09 (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB11 and repeat steps A thru E above.
- Next write 0A (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB10 and repeat steps A thru E above.

- Next write 0B (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB9 and repeat steps A thru E above.

- Next write 0C (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB8 and repeat steps A thru E above.

- Next write 0D (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB7 and repeat steps A thru E above.

- Next write 0E (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB6 and repeat steps A thru E above.

- Next write 0F (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB5 and repeat steps A thru E above.

- Next write 10 (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB4 and repeat steps A thru E above.

- Next write 11 (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB3 and repeat steps A thru E above.

- Next write 12 (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB2 and repeat steps A thru E above.

- Next write 13 (hex) to the Flash RAM Select register, to test the Digital Paddle board in module slot PB1 and repeat steps A thru E above.

CHECK OUT the Remainder of the VMEbus Registers

_____ Read the L2 Buffer Header word, under the "Decode L2 Header Word" **Option 12** in the VASE ADMEM Checkout Menu. The word should correctly report

_____ The slot address

_____ The board Serial Number (same as engraved number) programmed on **U17** page 16

_____ The Board Type (should be 003) programmed on **U26** page 16

_____ **Option 13** - Test the Pipeline Length Register. Located in the Pipeline FPGAs **U67-U71** (pages 16A-20A), and the L2 header FPGA **U28** (page 16B).

_____ **Option 14** - Test the Pipeline Offset Register. Located in the L2 Header FPGA **U27** (page 16B).

_____ **Option 15** - Test the DAC Data Register. Located in Café_Timing FPGA **U107** (page 25A).

_____ **Option 16** - Test the DAC Control Register. Located in Café_Timing FPGA **U107** (page 25A).

_____ **Option 17** - Test the CAFE Control Register. Located in Café_Timing FPGA **U107** (page 25A).

_____ **Option 18** - Test the CAFE Delay Register. Located in Café_Timing FPGA **U107** (page 25A).

_____ **Option 19** - Test the Channels (0-3) Pedestal Subtraction Register. Located in Pipeline FPGA **U71** (page 16A).

_____ **Option 20** - Test the Channels (4-7) Pedestal Subtraction Register. Located in Pipeline FPGA **U70** (page 17A).

_____ **Option 21** - Test the Channels (8-11) Pedestal Subtraction Register. Located in Pipeline FPGA **U69** (page 18A).

_____ **Option 22** - Test the Channels (12-15) Pedestal Subtraction Register. Located in Pipeline FPGA **U68** (page 19A).

_____ **Option 23** - Test the Channels (16-19) Pedestal Subtraction Register. Located in Pipeline FPGA **U67** (page 20A).

_____ **Option 24** - Run an Overnight loop on the ADMEM registers for at least 1000 loops.

Check PLLs

_____ Insert the Testclk Module into slot 4. The TESTCLK jumpers should be set to allow for the backplane clock to be driven.

_____ Turn on the Backplane clock on the TESTCLK.

_____ Observe the following pins on **U65: 10 (TP 113) , 11 (TP 90) , 14 (TP 92) , 15 (TP 91)** (page 4). You should observe a 132 ns clock with 50%duty cycle (66ns up, 66ns down) at these pins.

_____ Observe **U65-20 (TP 89).** You should observe a 66 ns clock with 50%duty cycle (33ns up, 33ns down) at these pins.

_____ Observe the following pins on **U103: 11, 15** (page 25). You should observe a 132 ns clock with 50%duty cycle (66ns up, 66ns down) at these pins.

_____ Observe **U103-20.** You should observe a 66 ns clock with 50%duty cycle (33ns up, 33ns down) at these pins.

Check of Diagnostic Mode Data thru Trigger Sums

In this test we will pump data from the Diagnostic FIFO into the Pipeline FPGAs. This diagnostic data will be used in place of the data normally coming from CAFÉ modules.

_____ The Testclk Module is needed for this test. The TESTCLK jumpers should be set to allow for the backplane clock to be driven.

_____ Connect the TSCR's top port to the ADMEM's top port.

_____ Select **Option 25 - Diagnostic Mode Data Test**

This test is done automatically, user needs to check screen for errors and verification of the below steps:

- Turn on the Backplane clock on the TESTCLK.
- Turn on the TSIE Backplane Enable. (If TRACER is being used, the Cable clock will be used.)
- Turn on the TSIE Wait.
- Set the five ADMEM Trigger Sum Subtraction Pedestal Registers to zero.
- set the Pipeline depth to 2A (hex)
- set the Pipeline offset to 03 (hex)
- select all channels in the Pipeline Diagnostic Channles Enable Register - (toggle to high)
- select MC Phase Delay
- Send the tsi pattern /home/usr2/projects/software/send_halt.tsi
- clear the Diagnostic FIFO by issuing a software reset in the Control Register
- Fill the Diagnostic data with sequential data
- Turn on the "Enable Diagnostic Pipeline Data" bit in the Control Register.
- Through the TESTCLK send the tsi pattern /home/usr2/projects/software/h_r_r.tsi
- The TSCR will capture the diagnostic data, and check it for accuracy.
- Next follow the instructions in VASE as all seven ADMEM ports are checked.

Check the readout of the Digital Pipeline thru L2 buffers and L1 pipeline

In this test we will pump data from the Diagnostic FIFO into the Pipeline FPGAs. This diagnostic data will be used in place of the data normally coming from CAFÉ modules.

_____ The Testclk Module is needed for this test. The TESTCLK jumpers should be set to allow for the backplane clock to be driven.

_____ Select **Option 26 - Diagnostic Mode Data Test**

This test is done automatically, user needs to check screen for errors and verification of the below steps:

- Turn on the Backplane clock on the TESTCLK.
- Turn on the TSIE Backplane Enable.
- Turn on the TSIE Wait.
- Send the tsi pattern /home/usr1/tshaw/test_admem/send_halt.tsi
- set the Pipeline depth to 2A (hex)
- set the Pipeline offset to 03 (hex)
- select all channels in the Pipeline Diagnostic Channles Enable Register - (toggle to high)
- clear the Diagnostic FIFO by issuing a software reset in the Control Register
- Fill the Diagnostic data with sequential data
- Turn on the “Enable Diagnostic Pipeline Data” bit in the Control Register.
- From the TESTCLK send the tsi pattern /home/usr2/projects/software/diag_fifo_test.tsi
- At the ADMEM, Dump the L2 buffer information, the data you get should match the following hi-lited text:

Channel L2 Buffer 0 L2 Buffer 1 L2 Buffer 2 L2 Buffer 3

Header	0000138**2**	0000138**3**	0000138**4**	0000138**5**
0	**01C2**	**01C3**	**01C4**	**01C5**
1	**01C2**	**01C3**	**01C4**	**01C5**
2	**01C2**	**01C3**	**01C4**	**01C5**
3	**01C2**	**01C3**	**01C4**	**01C5**
4	**01C2**	**01C3**	**01C4**	**01C5**
5	**01C2**	**01C3**	**01C4**	**01C5**
6	**01C2**	**01C3**	**01C4**	**01C5**
7	**01C2**	**01C3**	**01C4**	**01C5**
8	**01C2**	**01C3**	**01C4**	**01C5**
9	**01C2**	**01C3**	**01C4**	**01C5**
10	**01C2**	**01C3**	**01C4**	**01C5**
11	**01C2**	**01C3**	**01C4**	**01C5**
12	**01C2**	**01C3**	**01C4**	**01C5**
13	**01C2**	**01C3**	**01C4**	**01C5**
14	**01C2**	**01C3**	**01C4**	**01C5**
15	**01C2**	**01C3**	**01C4**	**01C5**
16	**01C2**	**01C3**	**01C4**	**01C5**
17	**01C2**	**01C3**	**01C4**	**01C5**
18	**01C2**	**01C3**	**01C4**	**01C5**
19	**01C2**	**01C3**	**01C4**	**01C5**

Directly following the above test,

- At the TESTCLK, Send the tsi pattern /home/usr2/projects/software/send_halt.tsi
- At the ADMEM, Set the “Enable VMEbus Read of Pipeline data” bit in the Control register
- Now select the ADMEM Register option, which allows you to view the contents of the digital pipeline.

  Look at all 20 channels.

  They should contain identical data which is incremented by 1 count for each word.

Check of the Digital Pipeline data with Digital Paddle Cards

For this test, a TESTCLK (capable of driving the backplane clock) must be in the crate.

The ADMEM module must have digital Paddle cards loaded in all 20 slots. The digital Paddle cards should have sequential data loaded in them.

_____ First load the ADMEM with Digital Paddle Boards which have been downloaded **with sequential data**.

_____ Run the TAM program for at least 20,000 loops.

_____ Now load the ADMEM with Digital Paddle cards which have been loaded **with pattern data** (AAAA,55555,0000,FFFF)

_____ Run the TAM Program for at least 20,000 loops.

Quick Check of the Trigger Sums – Low Order Bits

From VASE in the Checkout Menu, select **Option 27** - Pipeline Trigger Sum Test- Low Order Bits. Prior to running the test, connect the trigger sum cable as stated below. Thereafter, the program will prompt user to either continue test or quit. At that time the user should change the cable as necessary.

The following test, tests the 10 least significant bits of the Trigger Sums, (9:0)

This test requires the use of a TESTCLK and TSCR.

_____ Connect a trigger sum cable from the top (first) connector to the top (first) connector of the TSCR board.

_____ Follow test instructions within VASE.

(Vase will help perform the below processes)

- ADMEM must be configured as a PLUG ADMEM for this test.
- The TESTCLK jumpers should be set to allow for the backplane clock to be driven.
- Turn on the Backplane clock on the TESTCLK.
- Turn on the TSIE Backplane Enable.
- ADMEM setup, the program will do this,
- Turn on Trigger Sum Pass-through mode,
- Fill Trigger Sum Flash RAM with sequential data,
- fill CAFÉ Slots with “sequential data” digital paddle boards
- TSCR setup,
- from the Control Register, reset the FIFOs
- make sure VMEbus access to the FIFOs is NOT enabled (should be zero).
- From the TESTCLK TSI menu, send the tsi pattern /people/tshaw/test_admem/h_r_r.tsi
- Now at the TSCR, use the Control Register to enable VMEbus access to the FIFOs
- Note that the TSCR FIFOs should all read Full
- Go to the TSCR FIFO access menu, use option 8 to read out locations.

Quick Check of the Trigger Sums – High Order Bits

The following procedure will test the most significant 10 bits, (15:6).

From VASE in the Checkout Menu, select **Option 28** - Pipeline Trigger Sum Test-High Order Bits. Prior to running the test, connect the trigger sum cable as stated below. Thereafter, the program will prompt user to either continue test or quit. At that time the user should change the cable as necessary.

This test requires the use of a TESTCLK and TSCR.

_____ Connect a trigger sum cable from the top (first) connector to the top (first) connector of the TSCR board.

_____ Follow test instructions within VASE.

(Vase will help perform the below processes)

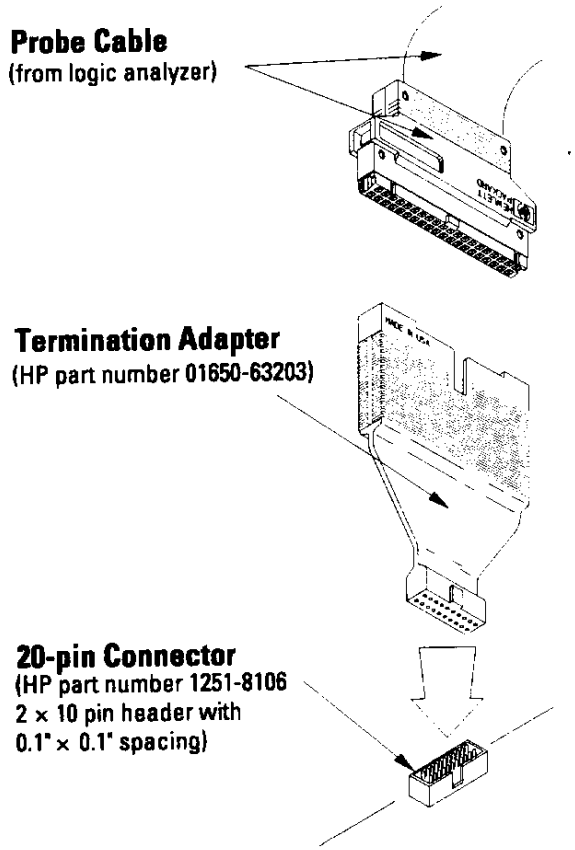
- ADMEM must be configured as a PLUG ADMEM for this test.
- The TESTCLK jumpers should be set to allow for the backplane clock to be driven.
- Turn on the Backplane clock on the TESTCLK.
- Turn on the TSIE Backplane Enable.
- ADMEM setup, the program will do this,
- Turn on Trigger Sum Pass-through mode,
- Fill Trigger Sum Look-up Flash RAM with **sequential data Divided by 32**,
- fill CAFÉ Slots with “sequential data” digital paddle boards
- TSCR setup,
- from the Control Register, reset the FIFOs
- make sure VMEbus access to the FIFOs is NOT enabled (should be zero).
- From the TESTCLK TSI menu, send the tsi pattern /people/tshaw/test_admem/h_r_r.tsi
- Now at the TSCR, use the Control Register to enable VMEbus access to the FIFOs
- Note that the TSCR FIFOs should all read Full
- Go to the TSCR FIFO access menu, use option 8 to read out locations.

Test of Signals from Mezzanine Card

The following tests make use of a specially adapted Digital Paddle Board with special test points.

Logic Analyzer Port - On the Digital Paddle Board

Tracer Front Panel Ports J will provide ports for easy access to the CDF backplane trigger and clock signals. These ports will bring TTL level signals to four 20 pin right angle box headers on the front panel. The ports can be used by a wide range of oscilloscopes or logic analyzers, but are specifically designed for ease of use with HP logic analyzers and the HP Terminator Adapter.



Hewlett Packard Pinout on Terminator Adapter (HP part number 01650-63203)

Pin	Signal	Pin	Signal
20	GND	19	D0
18	D1	17	D2
16	D3	15	D4
14	D5	13	D6
12	D7	11	D8
10	D9	9	D10
8	D11	7	D12
6	D13	5	D14
4	D15	3	CLK1
2	CLK2	1	+5V

CDF Signals are connected to the Port as follows:

Digital Test Card Port J3 (TOP) - Connect to LA POD 1

Pin	Signal	Pin	Signal
20	GND	19	***FRAM_IO(0)***
18	***FRAM_IO(1)***	17	***FRAM_IO(2)***
16	***FRAM_IO(3)***	15	***FRAM_IO(4)***
14	***FRAM_IO(5)***	13	***FRAM_IO(6)***
12	***FRAM_IO(7)***	11	***FRAM_IO(8)***
10	***FRAM_IO(9)***	9	***FRAM_IO(10)***
8	***FRAM_IO(11)***	7	***FRAM_IO(12)***
6	***FRAM_IO(13)***	5	***FRAM_IO(14)***
4	***FRAM_IO(15)***	3	No Connect
2	No Connect	1	+5V

Digital Test Card Port J2 (MIDDLE) - Connect to LA POD 2

Pin	Signal	Pin	Signal
20	GND	19	***FRAM_ADDR(0)***
18	***FRAM_ADDR(1)***	17	***FRAM_ADDR(2)***
16	***FRAM_ADDR(3)***	15	***FRAM_ADDR(4)***
14	***FRAM_ADDR(5)***	13	***FRAM_ADDR(6)***
12	***FRAM_ADDR(7)***	11	***FRAM_ADDR(8)***
10	***FRAM_ADDR(9)***	9	***FRAM_ADDR(10)***
8	***FRAM_ADDR(11)***	7	***FRAM_ADDR(12)***
6	***FRAM_ADDR(13)***	5	***FRAM_ADDR(14)***
4	***FRAM_ADDR(15)***	3	No Connect
2	No Connect	1	+5V

Digital Test Card Port J4 (BOTTOM) - Connect to LA POD 3

Pin	Signal	Pin	Signal
20	GND	19	***EXT_CONTROL****
18	***FRAM_WE****	17	***CAFÉ_OUT_CLK***
16	***CAFÉ_ADC_CLK***	15	***CAFÉ_QIE_RST***
14	***CAFÉ_QIE_CLK***	13	***CAFÉ_CAL_EN***
12	***CAFÉ_SMON_EN***	11	***CAFÉ_PATH_SEL***
10	No Connect	9	No Connect
8	No Connect	7	No Connect
6	No Connect	5	No Connect
4	No Connect	3	No Connect
2	No Connect	1	+5V

TESTCLK **Port J4 - Connect to LA POD 4**

Pin	Signal	Pin	Signal
20	GND	19	***CDF_CALEN****
18	CDF_RowA25	17	CDF_RowC26
16	***CDF_ERROR****	15	***CDF_L2R****
14	***CDF_L2A****	13	***CDF_L2A_EN****
12	***CDF_L2BD0****	11	***CDF_EVID0****
10	CDF_RowA29	9	***CDF_EVID1****
8	***CDF_L2BD1****	7	***CDF_EVID2****
6	***CDF_RSVD0****	5	***CDF_EVID3****
4	***CDF_RSVD1****	3	CDF_CLOCK
2	No Connect	1	No Connect

_____ Select **Option 29** and verify the following:

_____ With the Special Digital Paddle Board inserted in PB20, observe the signals CAFÉ_PATH_SEL, CAFÉ_SMON_ENABLE, and CAFÉ_CAL_EN1.

_____ Writing to the CAFÉ Control register, verify that you can

- _____ Toggle CAFÉ_PATH_SEL
- _____ Toggle CAFÉ_SMON_ENABLE
- _____ Toggle CAFÉ_CAL_EN1 (observe CAFÉ_CAL_EN)

_____ Move the Special Digital Paddle Board to PB15.

- _____ Toggle CAFÉ_CAL_EN2 (observe CAFÉ_CAL_EN)

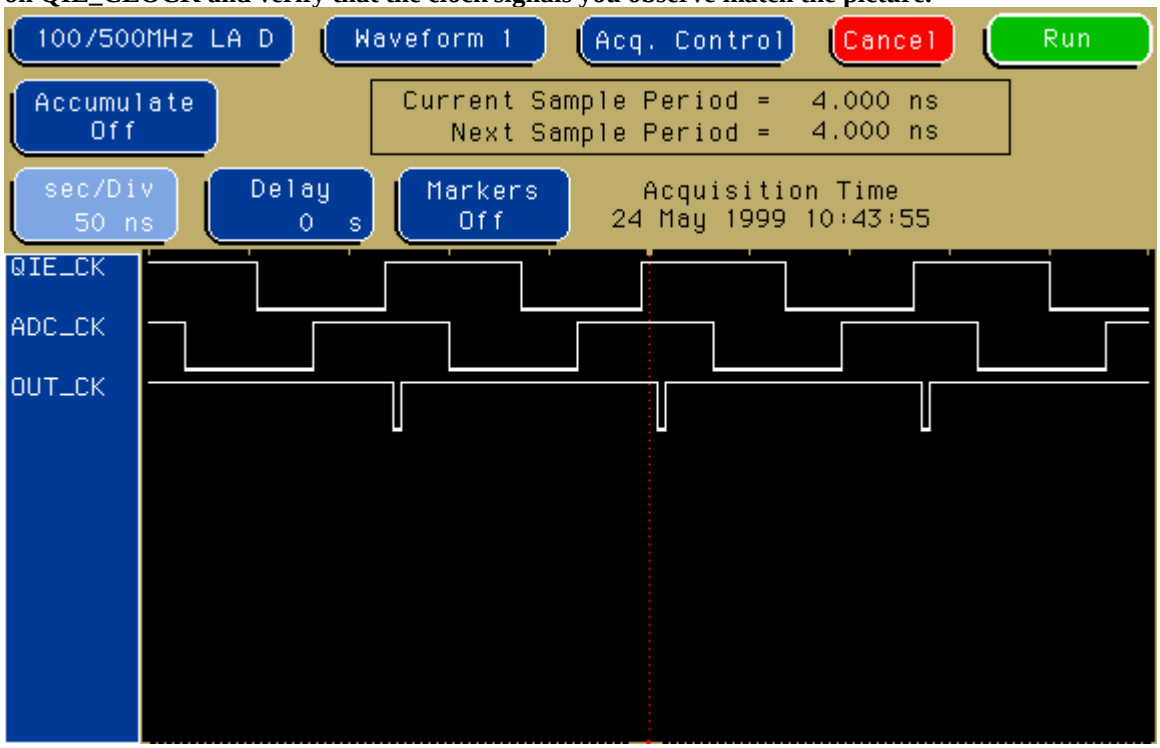
_____ Move the Special Digital Paddle Board to PB10.

- _____ Toggle CAFÉ_CAL_EN3 (observe CAFÉ_CAL_EN)

_____ Move the Special Digital Paddle Board to PB5.

- _____ Toggle CAFÉ_CAL_EN4 (observe CAFÉ_CAL_EN)

Now, with the TESTCLK driving the backplane clock, Observe the below signals. Trigger the LA on QIE_CLOCK and verify that the clock signals you observe match the picture.



NOTE: QIE_CK is CAFÉ_QIE_CLK
ADC_CK is CAFÉ_ADC_CLK
OUT_CK is CAFÉ_OUT_CLK

The Next step requires you observe the additional signals below.

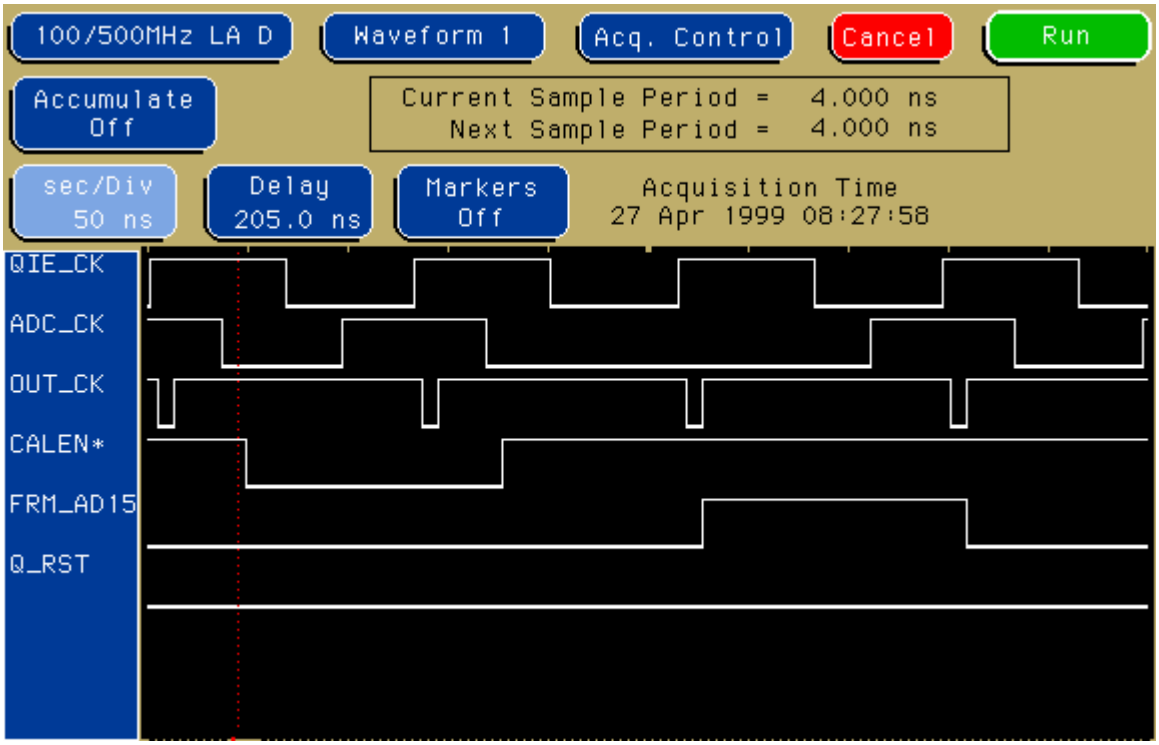
_____ Select **Option 30** to run a CAFÉ module calibration,

☐ The TESTCLK must be on, with the backplane clock running.

☐ The TSIE Backplane driver must be enabled.

☐ The TSI pattern /home/usr1/tshaw/test_admem/send_cal.tsi must be sent.

_____ You must trigger on the falling edge of CALEN* and should observe the following waveforms. NOTE the missing ADCCK* following a calibration.



NOTE:

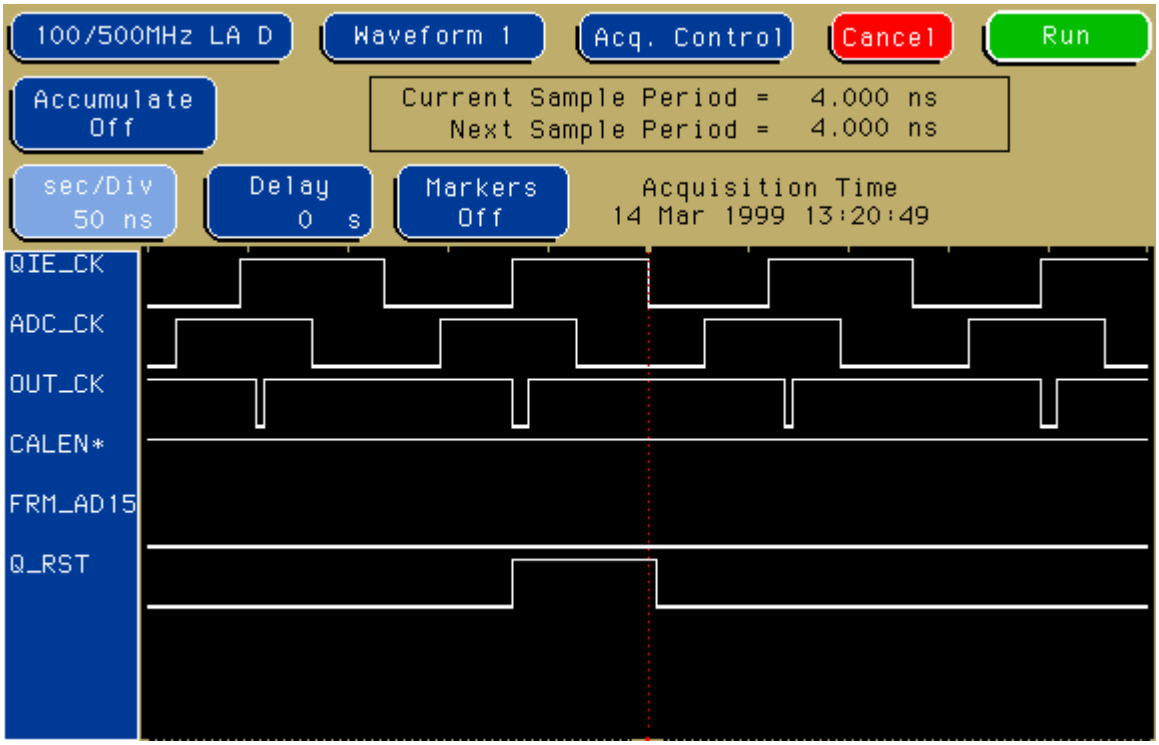
	QIE_CK	is	CAFÉ_QIE_CLK
	ADC_CK	is	CAFÉ_ADC_CLK
	OUT_CK	is	CAFÉ_OUT_CLK
	CALEN*	is	CDF_CALEN* (from Testclk)
	FRM_AD15	is	FRAM_ADDR(15)
	Q_RST	is	CAFÉ_QIE_RST

The Next step requires you observe the Q_RST signal to the CAFÉ modules.

_____ Select **Option 31** to do a CAFÉ module RESET

- The TESTCLK must be on, with the backplane clock running.
- The TSIE Backplane driver must be enabled.
- The TSI pattern /home/usr1/tshaw/test_admem/h_r_r.tsi must be sent.

_____ You must trigger on the falling edge of Q_RST and should observe the following waveforms.



NOTE:

	QIE_CK	is	CAFÉ_QIE_CLK
	ADC_CK	is	CAFÉ_ADC_CLK
	OUT_CK	is	CAFÉ_OUT_CLK
	CALEN*	is	CDF_CALEN* (from Testclk)
	FRM_AD15	is	FRAM_ADDR(15)
	Q_RST	is	CAFÉ_QIE_RST

Testing of the CAFÉ Delay Register

In this test we will verify the shifting of QIE_CLK with respect to CDF_CLK.

_____ Connect a Oscilloscope channel to CDF_QIE_CLK (**TP 113**) page 4 and set this channel up as the trigger.

_____ Connect a second Oscilloscope channel to **U105 – 15** (page 25). There should be a small (~7ns) shift in the second clock signal from the first.

_____ Now run **Option 32** in the ADMEM Checkout Procedure. This option will do a looping write of sequential data (0x0 to 0xFF) to the CAFÉ Delay Register. You should now see the second clock signal sweep across the first (trigger) signal.

Testing the DAC

To test the DAC on the mezzanine module, you **must be in a crate which provides the analog voltages**.

_____ Go to the ADMEM's functional submenu.

_____ Make sure the DAC is calibrated - DAC CAL OK should be high. If it is not, within the DAC Control Register
1) set the CS high,
2) set the CALIBRATE bit high,
3) set the CALIBRATE bit low,
4) then set the CS low

The DAC CAL_OK bit should now be high.

_____ Download a "0" to the DAC (option 4), and observe the voltage on pin 62 of a Café Module slot. The voltage should be around 0 volts.

_____ Download a "FFFF" to the DAC (option 4), and observe the voltage on pin 62 of a Café Module slot. The voltage should be around 10 volts.

_____ Download a "8000" to the DAC (option 4), and observe the voltage on pin 62 of a Café Module slot. The voltage should be around 5 volts.

_____ Finally, run **Option 33** – Test DAC of the ADMEM Checkout Menu and observe VCAL+. You should see this voltage ramping up from 0 to 10 volts.

Unresolved Tests Issues

How do we test connection of Analog signal to PB slots?

Check with real CAFE? requires Analog power